



Customer LDPC Order Form

The information in the Table below enables Avaliant to determine the service cost for each LDPC code, and simulation turnaround time. For instance, the total number of error blocks has a direct bearing on the simulation time. Accumulating 200 block errors will take twice as long as accumulating 100 errors. The turnaround time depends on when the simulation starts because the Avaliant LDPC Validator may be in use at the time. Volume orders receive discounts.

Please provide the following information about your LDPC code(s):

Parameters	LDPC Code #1	LDPC Code #2	***	LDPC Code #N
Rows/Columns of H matrix (see Figure 1)				
Number of edges of H matrix (see Figure 1)				
Modulation Type (DOCSIS 3.1) (BPSK, QPSK, 16QAM, 32QAM, 64QAM)				
Modulation BPSK with all-zero codeword ¹ (yes or no)				
Code Rate				
Number of Iterations (20, 30, 40, ...)				
Number of Error Blocks to Accumulate per SNR (100, 200, 300, 400, 500, ...)				
Lowest Block Error Rate ² (10^{-3} , 10^{-4} , 10^{-5} , 10^{-6} , ...)				
Lease number of points simulated on the BLER curves for every dB increment in channel SNR (see Figure 2) [4, 5, 6, etc.]				
LDPC Code Punctured (yes or no)				
LDPC Code Data Shortened (yes or no)				
LLR algorithm (Approximate or Exact)				
Received symbol Quantized (no or how many bits)				

¹ BPSK with all zero codeword allows the customer to strictly optimize LDPC codes

² In Figure 2, the lowest BLER is 10^{-6}



$$H = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 1 & 0 & 1 & 1 & 1 \\ 1 & 1 & 0 & 0 & 1 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 & 1 & 1 & 1 & 0 \end{pmatrix}$$

Rows of H: 4
Columns of H: 8
Number of Edges: 24

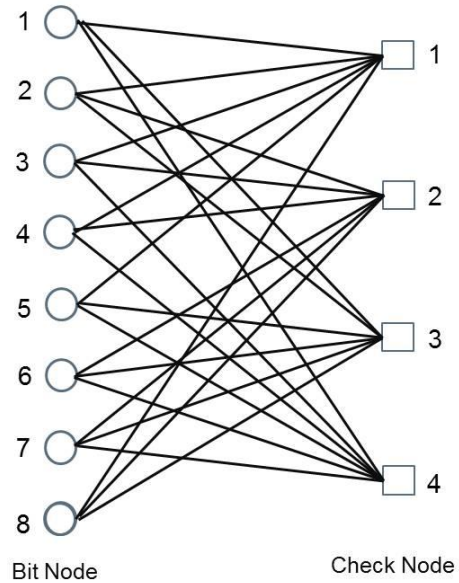


Figure 1: Example of H Matrix Rows, Columns, and Edges

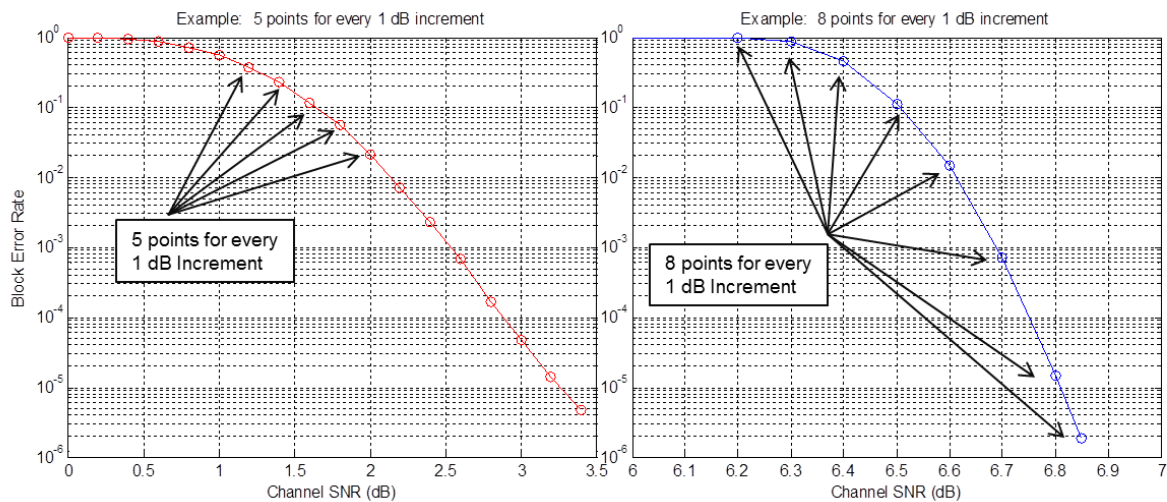


Figure 2: Example of 5 and 8 points for every 1 dB BLER increment

About Avaliant

Avaliant is a world-class solutions provider based in Bellevue, Washington. For more information about Avaliant, please visit us at www.avaliant.com